What is claimed is:

1. A random access memory device in an integrated circuit chip, comprising:

a memory array of memory cells organized into rows and columns, including a plurality of word lines and bit lines, each row of memory cells being coupled to a word line and each column of memory cells being coupled to a bit line;

sense amplifier circuitry coupled to the bit lines and being selectively disabled;

address decode circuitry for receiving an address value and asserting a row line associated therewith; and

test circuitry, coupled to at least one bit line, for placing on an external pad of the integrated circuit chip a current level corresponding to a voltage level appearing on the at least one bit line, while concurrently disabling the sense amplifier circuitry.

2. The random access memory device of claim 1, wherein the random access memory device comprises a ferroelectric memory device.

3. The random access memory device of claim 1, wherein the random access memory device comprises a nonvolatile memory device.

4. The random access memory device of claim 1, wherein the sense amplifier selectively drives the bit lines towards high and low reference voltage levels during normal memory access operations, the random access memory device is selectively configured in a test mode of operation by the test circuitry, and the sense amplifier circuitry is disabled from driving the bit lines by the test circuitry when the random access memory device is in the test mode of operation.

5. The random access memory device of claim 4, wherein the random access memory device includes a test input signal and is selectively configured in the test mode of operation based upon a value of the test input signal.

6. The random access memory device of claim 1, wherein the external pad is sized to contact and electrically connect to a tester probe, and the test circuitry comprises a pair of series-connected transistors coupled between the external pad and a reference voltage level, the pair of series-connected transistors including a first transistor having a control terminal coupled to the at least one bit line.

7. The random access memory device of claim 6, wherein the pair of series-connected transistors further comprises a second transistor having a control terminal connected to a control signal that selectively activates the second transistor.

8. The random access memory device of claim 1, wherein the external pad is sized to contact and electrically connect to a tester probe, and the test circuitry comprises a plurality of pairs of series-connected transistors coupled between the pad and a reference voltage level, each pair of series-connected transistors including a first transistor having a control terminal coupled to distinct bit line.

9. The random access memory device of claim 8, wherein each pair of series-connected transistors comprises a second transistor having a control terminal connected to a control signal that selectively activates the second transistor.

10. The random access memory device of claim 9, further comprising a selection circuit that selectively activates the second transistors of the plurality of pairs of series-connected transistors in a sequential manner.

11. The random access memory device of claim 10, wherein the selection circuit comprises counter circuitry and decode circuitry having a plurality of output signals such that each output signal is connected to the control terminal of a distinct second transistor.

12. The random access memory device of claim 1, wherein the test circuitry comprises:

a first pair of series-connected transistors connected between the external pad of the integrated circuit chip and a reference voltage level, a first transistor of the first pair of series-connected transistors having a control terminal connected to the at least one bit line; and

a second pair of series-connected transistors connected between a second pad of the integrated circuit chip and the reference voltage level, a first transistor of the second pair of series-connected transistors having a control terminal connected to a third pad of the integrated circuit chip and a second transistor of the second pair of series-connected transistors being activated.

13. The random access memory device of claim 1, further comprising:

calibration test circuitry for providing a relationship between the current level placed on the external pad and the voltage level appearing at the at least one bit line.

14. The random access memory device of claim 13, wherein the calibration test circuitry has substantially the same structure as a portion of the test circuitry.

15. The random access memory device of claim 13, wherein the calibration test circuitry comprises:

an input connected to a second external pad for externally controlling the operating characteristics of the calibration circuit; and

an output connected to a third external pad for externally measuring a current flowing through the calibration test circuitry.

16. A method of testing a semiconductor memory device having an array of memory cells and sense amplifier circuitry coupled to bit lines of the array, the semiconductor memory device being in an integrated circuit chip, the method comprising:

connecting memory cells in a row of memory cells to bit lines of the array;

disabling the sense amplifier circuitry from driving the bit lines;

selecting a bit line; and

providing a current level to a pad in the integrated circuit chip corresponding to a voltage level appearing on the selected bit line.

17. The method of claim 16, wherein:

the semiconductor memory device comprises a ferroelectric memory device.

18. The method of claim 16, further comprising measuring the current level provided to the pad.

19. The method of claim 16, further comprising:

repeating the steps of selecting and providing, with each step of selecting comprising selecting a different bit line in the array.

20. The method of claim 16, further comprising the step of:

determining a relationship between the current level provided to the pad and the voltage level appearing on the selected bit line; and

mapping the current level provided to a voltage level appearing across a memory cell connected to the selected bit line.

21. The method of claim 16, further comprising the steps of:

disconnecting the row of memory cells from the bit lines;

connecting another row of memory cells to the bit lines; and

repeating the steps of selecting and providing for the another row of memory cells.

22. An apparatus, comprising:

a random access memory device, comprising:

a memory array of memory cells organized into rows and columns, including a plurality of word lines and bit lines, each row of memory cells being coupled to a word line and each column of memory cells being coupled to a bit line;

address decode circuitry for receiving an address value and asserting a row line associated therewith; and

test circuitry, coupled to at least one bit line for placing on an external pad a current level corresponding to a voltage level appearing on the at least one bit line.

23. The apparatus of claim 22, wherein the random access memory device comprises a ferroelectric memory device.

24. The apparatus of claim 22, wherein the random access memory device comprises a nonvolatile memory device.

25. The apparatus of claim 22, wherein the random access memory device comprises sense amplifier circuitry that selectively drives the bit lines towards high and low reference voltage levels during normal memory access operations, the random access memory device is selectively configured in a test mode of operation by the test circuitry and the sense amplifier circuitry is disabled from driving the bit lines by the test circuitry when the random access memory device is in the test mode of operation.

26. The apparatus of claim 22, wherein the apparatus further comprises:

a processing unit having an address port connected to an address input port of the random access memory device and a data port connected to a data port of the random access memory device.

27. The apparatus of claim 22, wherein the external pad is sized to receive a tester probe, and the test circuitry comprises a pair of series-connected transistors coupled between the external pad and a reference voltage level, the pair of series-connected transistors including a first transistor having a control terminal coupled to the at least one bit line.

28. The apparatus of claim 27, wherein the pair of series-connected transistors further comprises a second transistor having a control terminal connected to a control signal that selectively activates the second transistor.

29. The apparatus of claim 22, wherein the external pad is sized to receive a tester probe, and the test circuitry comprises a plurality of pairs of series-connected transistors coupled between the external pad and a reference voltage level, each pair of series-connected transistors including a first transistor having a control terminal coupled to distinct bit line.

30. The apparatus of claim 29, wherein each pair of series-connected transistors comprises a second transistor having a control terminal connected to a control signal that selectively activates the second transistor.

31. The apparatus of claim 30, wherein the test circuitry comprises a selection circuit that selectively activates the second transistors of the plurality of pairs of series-connected transistors in a sequential manner.

32. The apparatus of claim 31, wherein the selection circuit comprises counter circuitry and decode circuitry having a distinct output signal connected to the control terminal of each of the second transistors.

33. The apparatus of claim 22, wherein the test circuitry comprises:

a first pair of series-connected transistors connected between the external pad of the apparatus and a reference voltage level, a first transistor of the first pair of series-connected transistors having a control terminal connected to the at least one bit line; and

a second pair of series-connected transistors connected between a second pad of the apparatus and the reference voltage level, a first transistor of the second pair of series-connected transistors having a control terminal connected to a third pad of the apparatus and a second transistor of the second pair of series-connected transistors being activated.

34. The apparatus of claim 22, wherein the random access memory device further comprises:

calibration test circuitry for providing a relationship between the current level and the voltage level appearing at the at least one bit line.

35. The apparatus of claim 34, wherein the calibration test circuitry has substantially the same structure as a portion of the test circuitry.

36. The apparatus of claim 34, wherein the calibration test circuitry comprises:

an input connected to a second external pad for externally controlling the operating characteristics of the calibration circuit; and

an output connected to a third external pad for externally measuring a current flowing through the calibration test circuitry.

37. An apparatus, comprising:

a ferroelectric capacitor; and

means for placing on an external pad of the apparatus a current level corresponding to a voltage level appearing across the ferroelectric capacitor.

38. The apparatus of claim 37, wherein the means for placing comprises a first transistor having a control terminal coupled to a plate of the ferroelectric capacitor, a first conduction terminal coupled to the external pad and a second conduction terminal coupled to a voltage reference.

39. The apparatus of claim 38, wherein the means for placing further comprises a second transistor series connected to the first transistor to form a pair of series connected transistors connected between the external pad and the voltage reference, and a means for selectively activating the second transistor.